

**FIG. 1**  
transceiver 10

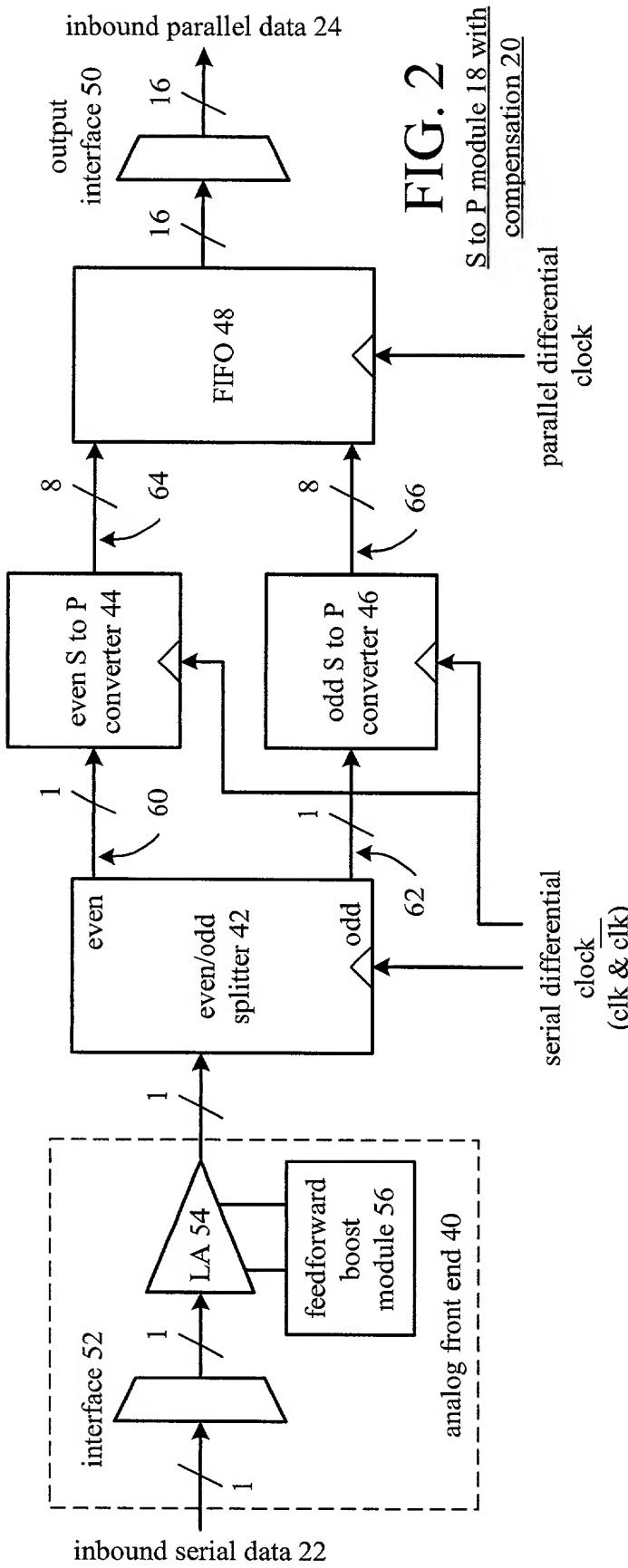


FIG. 2

S to P module 18 with compensation 20

parallel differential clock  
serial differential clock

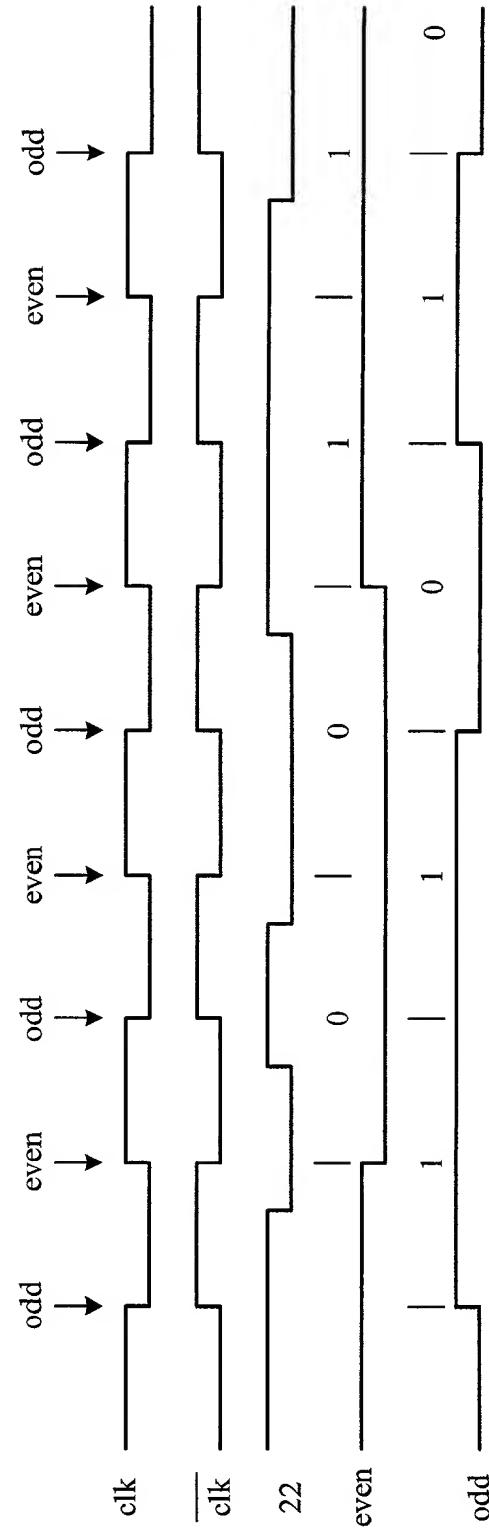


FIG. 3

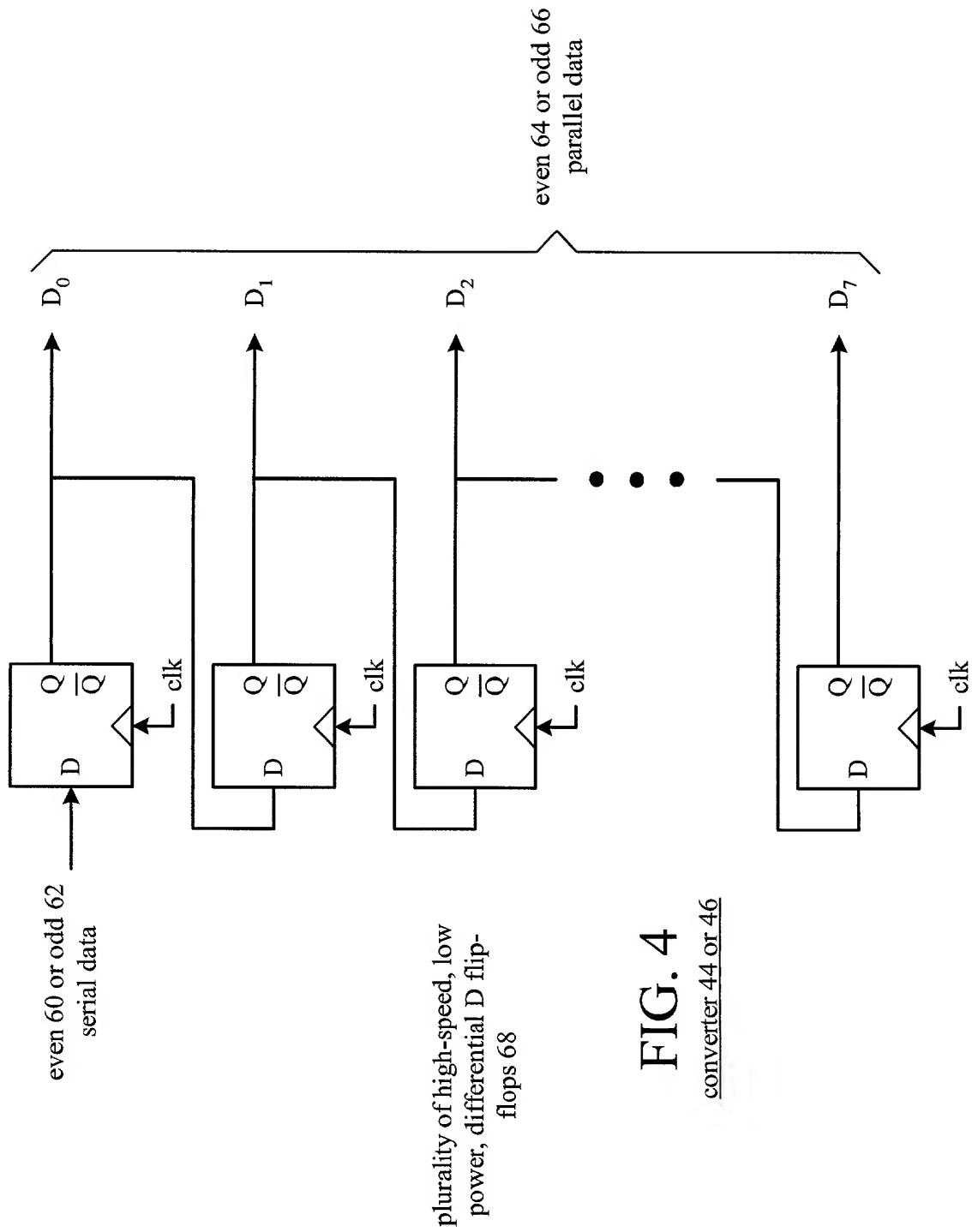


FIG. 4

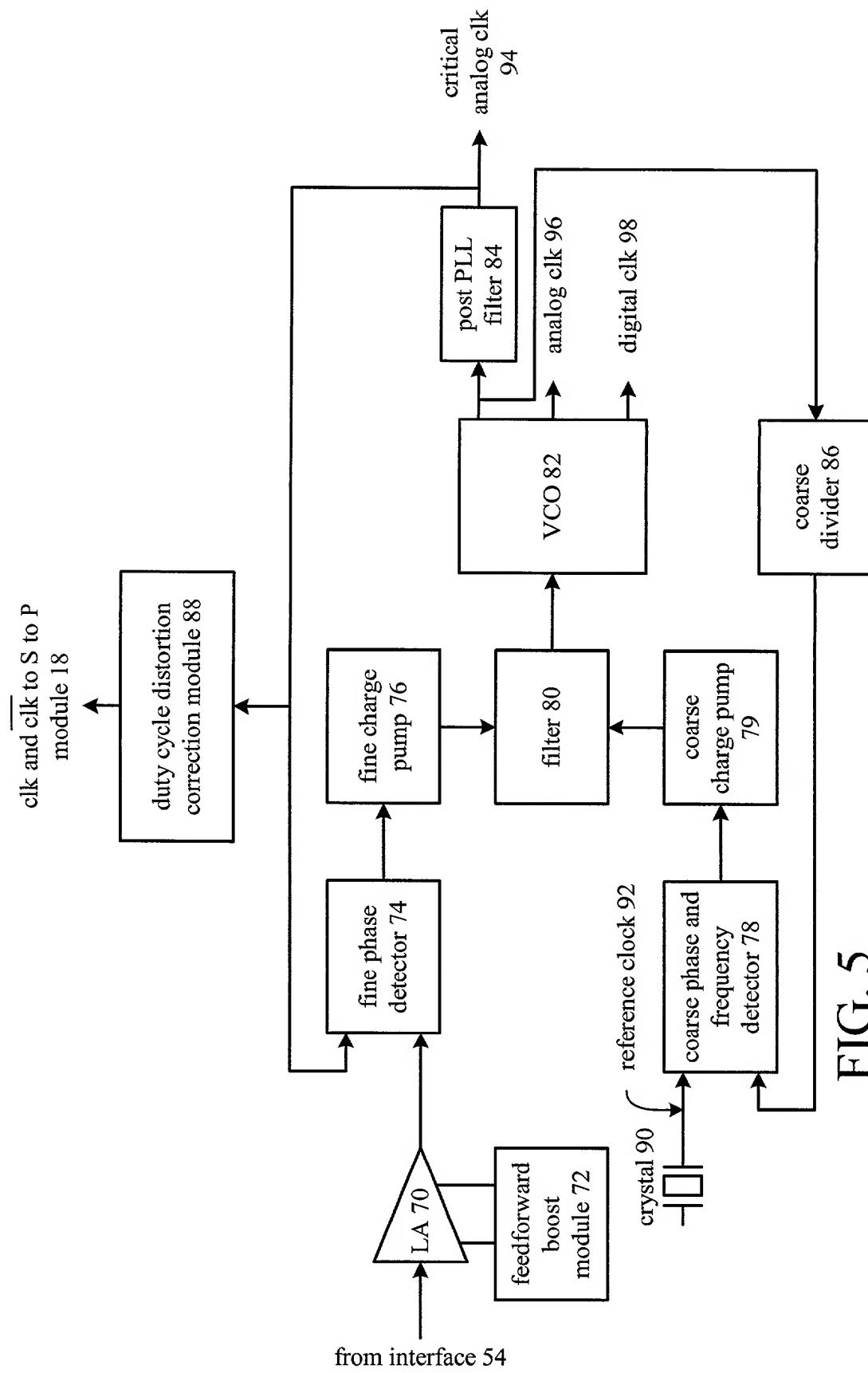
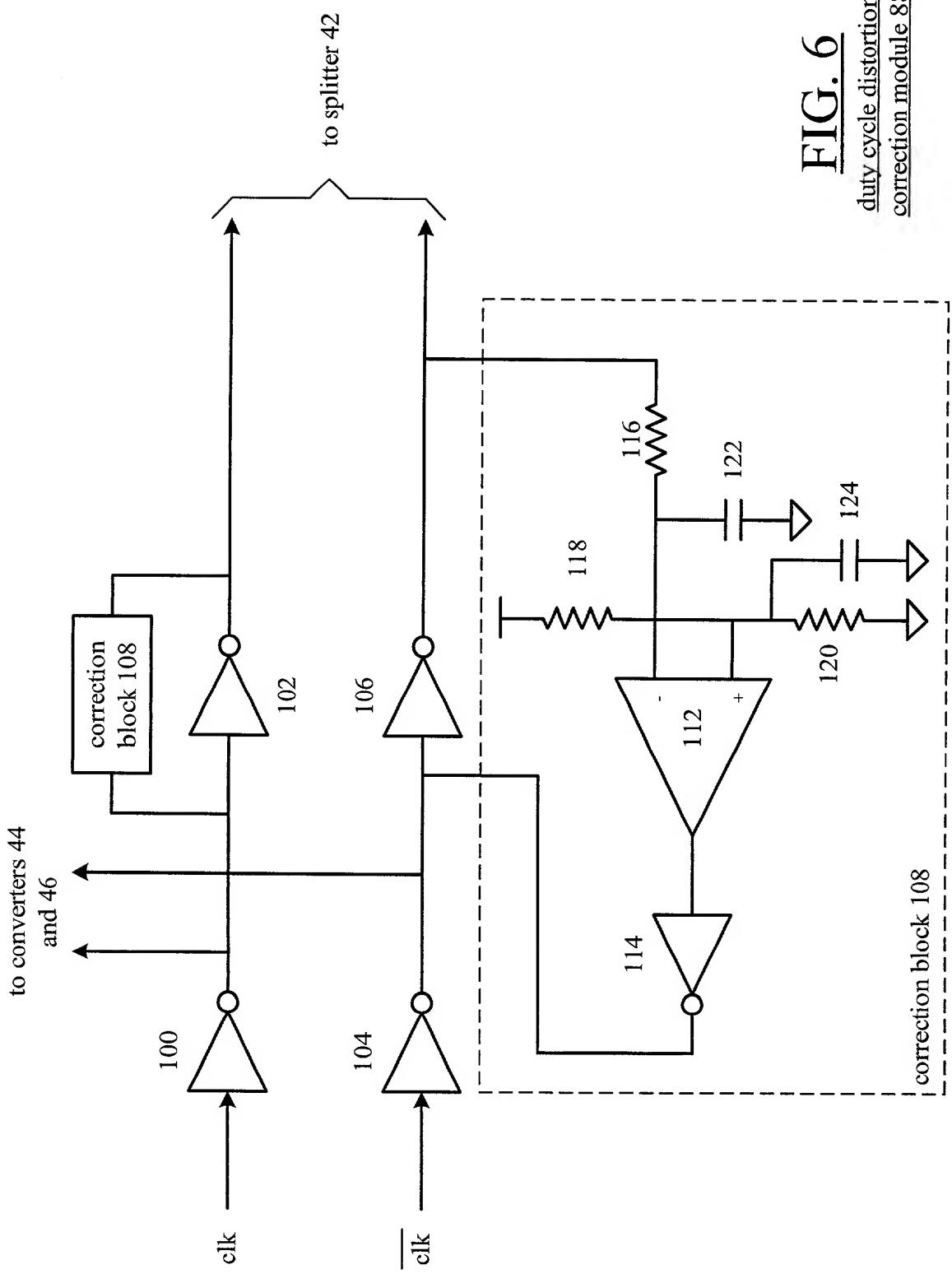


FIG. 5

Rx clocking circuit 16 with compensation 20



**FIG. 6**  
duty cycle distortion  
correction module 88

outbound serial data 36

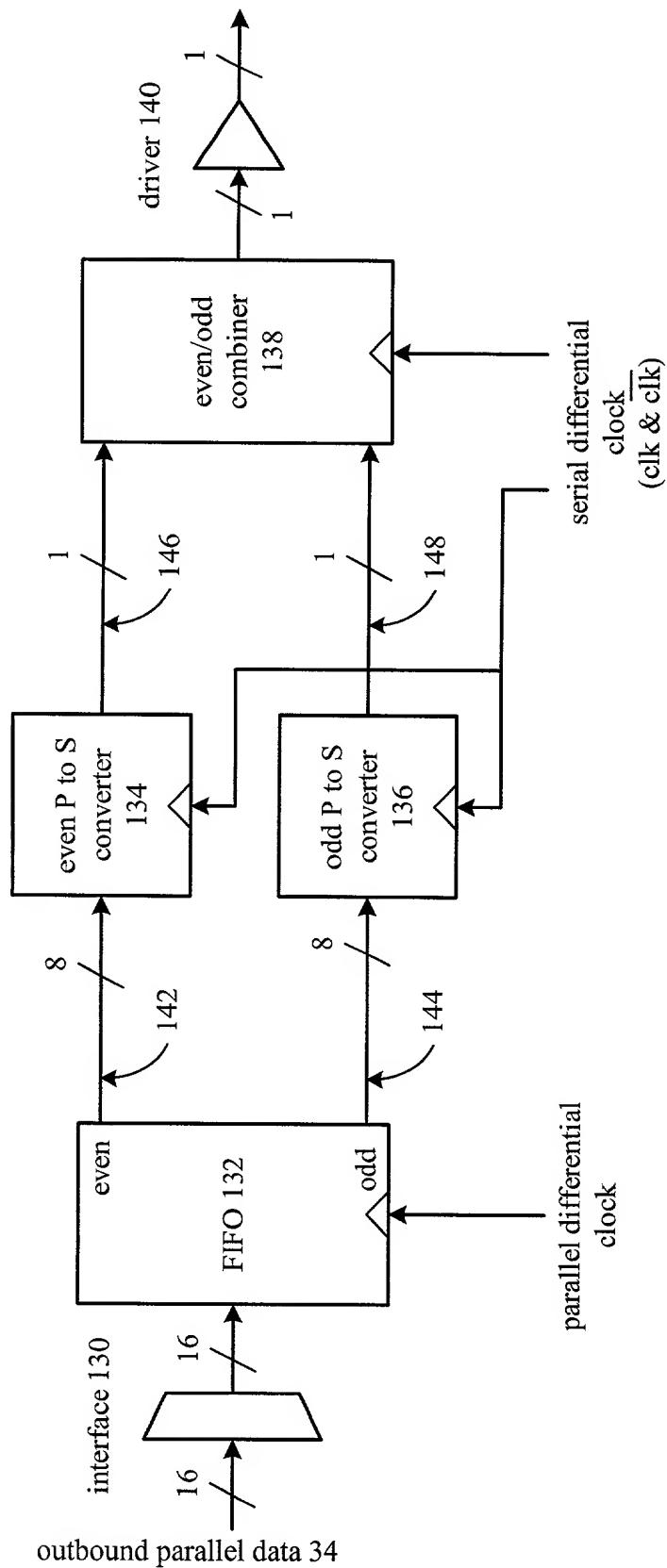
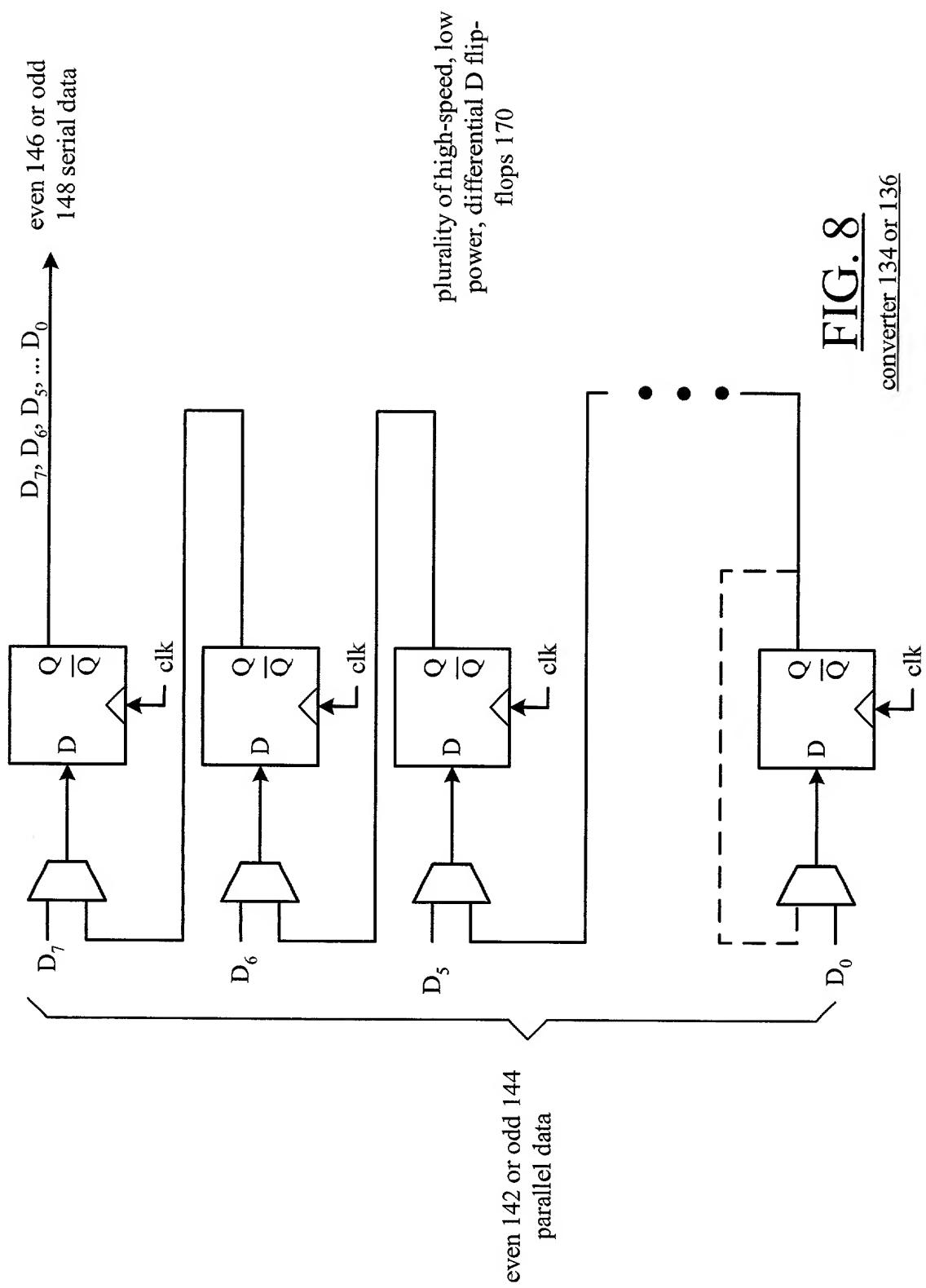


FIG. 7  
P to S module 30 with  
compensation 32



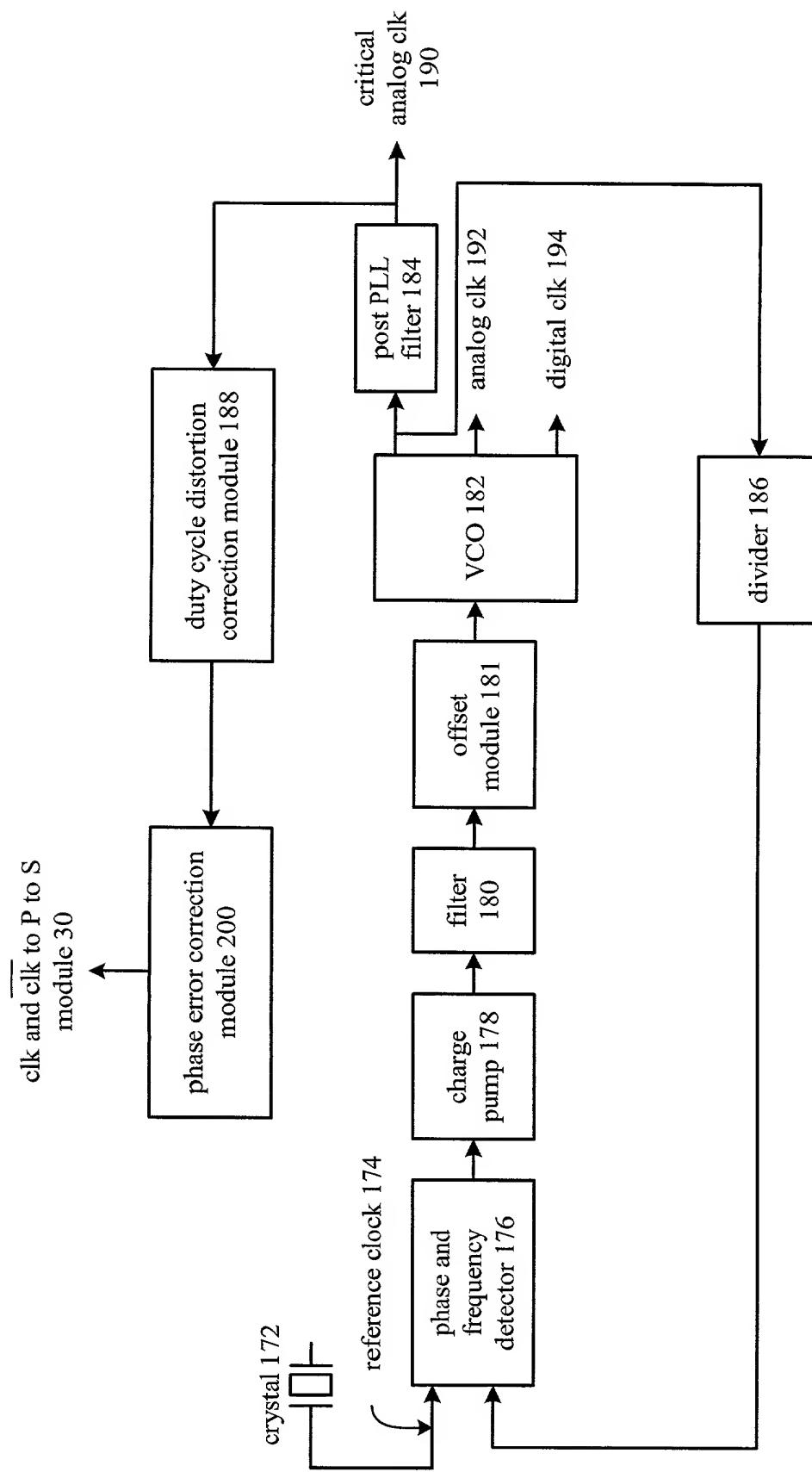


FIG. 9

Tx clocking circuit 28 with compensation 32

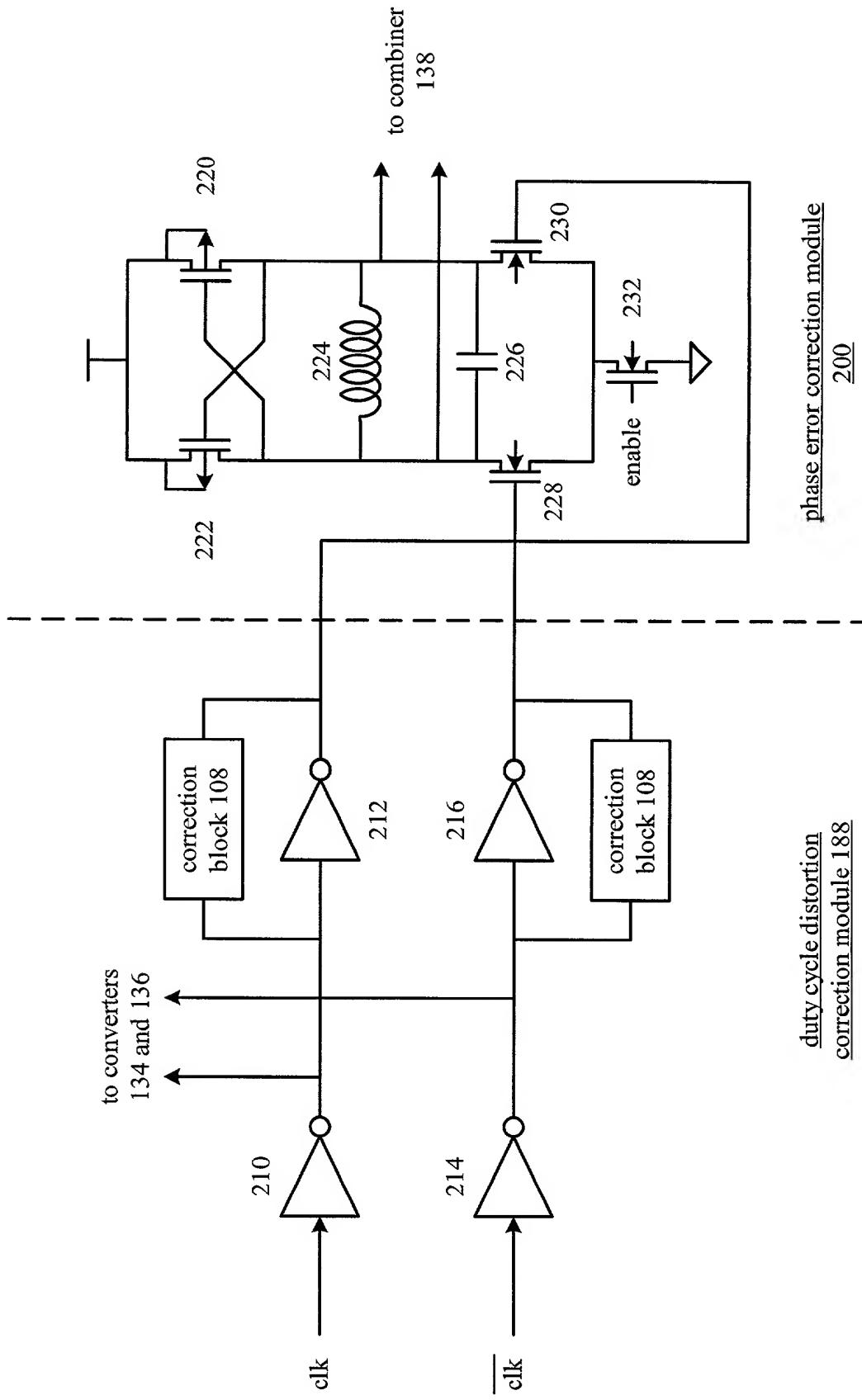


FIG. 10

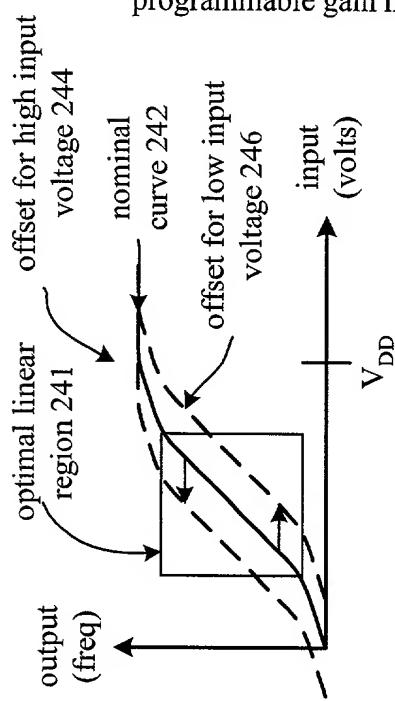


FIG. 11  
VCO curve

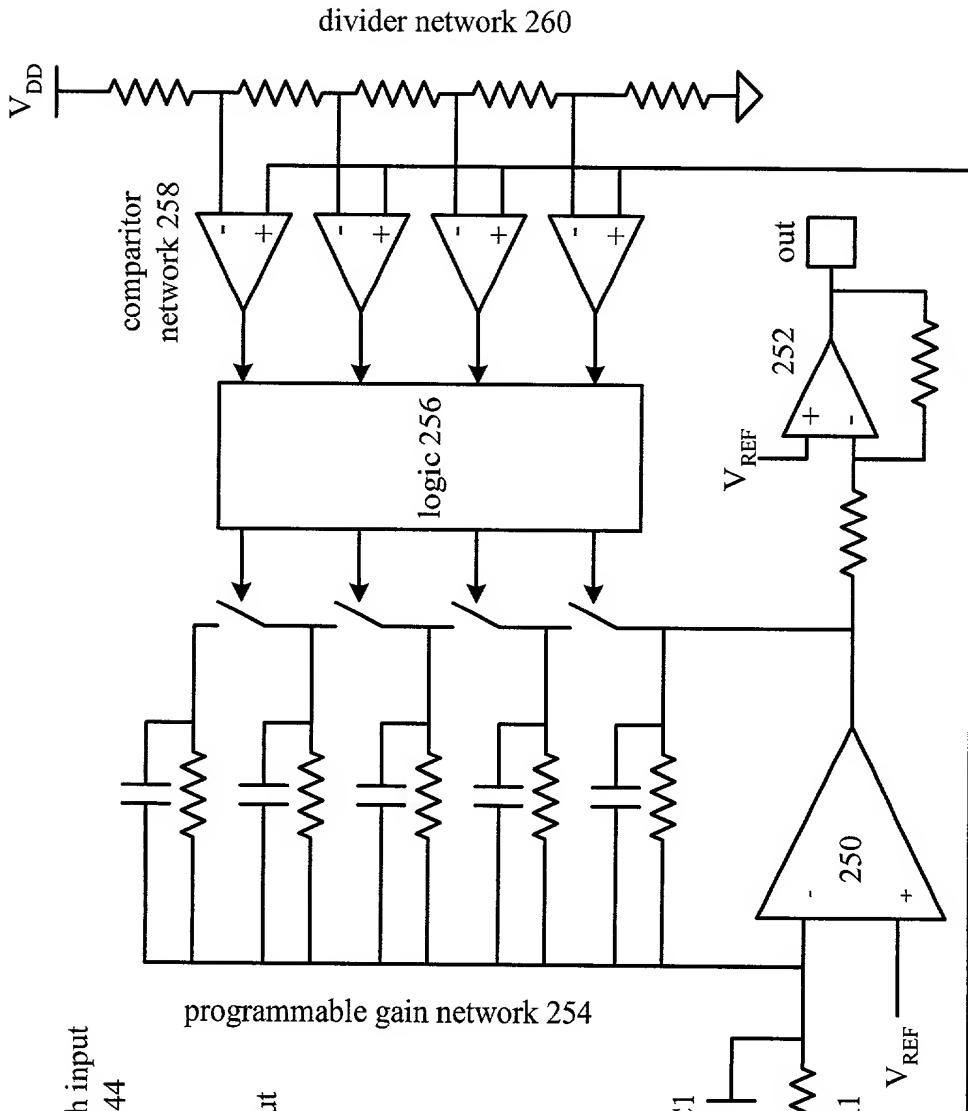
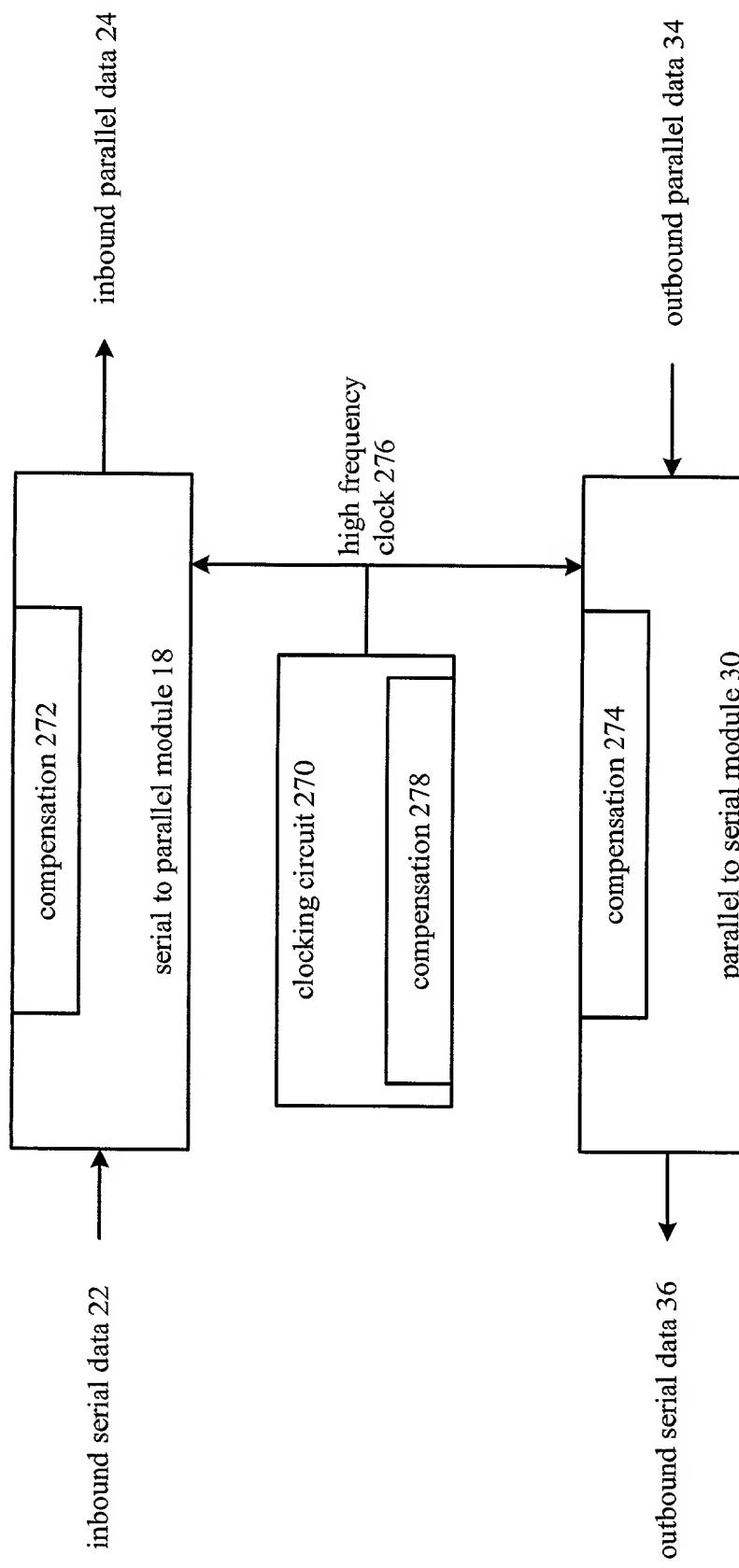


FIG. 12  
offset module 181



**FIG. 13**  
transceiver 275